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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,638	03/30/2001	Ryou Nakagaki	16869P-023300US	6928

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EXAMINER	
SHAPIRO, JEFFERY A	

ART UNIT	PAPER NUMBER
3653	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/823,638	NAKAGAKI ET AL.	
	Examiner	Art Unit	
	JEFFREY A. SHAPIRO	3653	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 5-10, 23-25, 27 and 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-10,23-25,27 and 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5-10, 23-25, 27 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berezin et al (US 5,539,752) in view of Stephan et al (US 6,338,001 B1) , further in view of Nishimura et al (US 5,761,337), further in view of Kumagai (US 5,394,481), further in view of Jarvis et al US 6,297,644 B1) and still further in view of Baker (US 5,226,118).

Berezin et al discloses the following.

As described in Claims 1, 6 and 9;

a. imaging an inspected semiconductor wafer object (32, 32a) (see col. 5, lines 45-60 and figure 1);

b. extracting an image of a defect candidate from an image obtained by said imaging step (see col. 6, lines 10-19);

c. classifying said extracted defect candidate image into a first category (20) (see figure 2 and col. 6, lines 32-64, noting defects are classed into the various types illustrated);

As further described in Claim 9;

d. said second category relating to predicted yield from said inspected object (32, 32a), (see col. 1, lines 35-42, col. 2, lines 27-38 and col. 8, .lines 24-33, which discuss predicting yield);

e. said first category in a map format (see col. 1, lines 5-12, which mentions that Berezin's apparatus performs map analysis of wafer defects, i.e, map format.)

Berezin further discloses as described in Claims 7, 10 and 23-25, the imager is a scan mechanism (40) which includes microscope, which is construed as meaning an electron microscope, since this is the predominant microscope for use in detecting semiconductor wafer defects.

Further regarding Claims 1, 6 and 9, Berezin et al discloses as follows:

f. displaying on a screen said extracted defect candidate image *together with first and second classification information, said first classification information relating to* said first category, *said second classification information relating to* said second category;

g. *said step of classifying said extracted defect candidate image into said second category is performed by comparing a circuit pattern area and a defect area, said circuit pattern area being obtained from a reference image and said defect area being obtained from said imaging step*;

See Berezin et al, figures 1, 2 and 4. Figure 1 illustrates a display with computers (36 and 16). These displays are discussed as having various defect images that can be compared through preclassification and analysis programs (20, 22), as described in col. 6, lines 5-19 and 45-64.

Berezin does not expressly disclose the use of kill ratio data as a comparison criteria for displaying along with defect image and classification data, for example. However, Stephan discloses using kill ratio data (112, 310) in analyzing semiconductor wafer defects.

At the time of the invention, it would have been obvious for one ordinarily skilled in the art to have included kill ratio data in Berezin's display screens.

The suggestion/motivation would have been because one ordinarily skilled in the art would have recognized based upon Berezin's disclosure, as described above, that effective review and comparison of the chip defects would be enhanced by use of kill ratio data, as taught by Stephan. See Stephan, col. 1, line 59-col. 2, line 10, col. 4, lines 65-67 and col. 5, lines 1-10.

Berezin discloses the system described above. Berezin does not expressly disclose, but Nishimura et al, Kumagai and Jarvis disclose the following;

As described in Claims 1, 5, 6, 8, 9, 27 and 33;

h. said defect type includes one or more of the following: particle defects, flaw defects, circuit pattern short defects, circuit pattern open defects and voltage contrast defects; (Kumagai, fig.9, Jarvis, col. 1, line 65-col. 2, line 10, and Nishimura, figure 3.)

As described in Claims 1, 5, 9 and 33;

i. calculating third information relating to voltage contrast of the defect candidate; (Jarvis, abstract, col. 13, line 52-col. 14, line 8 and figure 11.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have inspected a wafer for particle defects, flaw defects, circuit pattern short defects, circuit pattern open defects and voltage contrast defects as described in Claims 1, 5, 6, 8, 9, 27 and 33.

The suggestion/motivation would have been to obtain defect information on semiconductor wafer defects. See Berezin, col. 6, lines 45-64.

Note that figure 9 of Kumagai discloses various types of defects charted, such as holes, spots and breaks that fall into the categories of particle defects, flaw defects. Kumagai also discloses breaks, which can be construed as circuit pattern open defects, as described in section “h” above. Figure 3 of Nishimura discloses images of various connection faults and short circuits, said short circuits and connection faults construed as voltage contrast defects, as described in section “h and i” above. Note that an inspection system such as that of Berezin et al determines such defects, as one ordinarily skilled in the art would recognize them as well-known semiconductor circuit defects found in wafers during manufacturing.

Therefore, one ordinarily skilled in the art would have found it obvious in light of the teachings of Kumagai and Nishimura to chart and display as well as compare this various data on Berezin's displays.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have calculated third information related to voltage contrast defects as described in Claims 1, 5, 9 and 33.

The suggestion/motivation would have been to obtain defect information on semiconductor wafer defects. See again, Berezin, col. 6, lines 45-64.

Regarding Claims 1, 5, 9 and 33, note that Jarvis discloses and teaches actual testing equipment and techniques regarding detection of voltage contrast flaws by flowing electrons through the circuits and obtaining voltage readings for comparison with expected voltages. See Jarvis et al (US 6,297,644), last four lines of abstract and figures 9a, 9b, 10a, 10b and 11, illustrating short circuit situations and col. 2, lines 66 and 67, col. 3, lines 1-9, and col. 7, lines 58-col. 8, line14, mentioning use of a scanning electron microscope (SEM) to perform such voltage contrast studies of defects. Therefore, based on Jarvis' teaching, it would have been obvious for one ordinarily skilled in the art to have used Berezin's SEM to obtain voltage contrast information and then to have calculated third information data relating to said voltage contrast for a particular wafer.

Regarding Applicant's newly added claim language to Claim 1

"displaying on a screen said extracted plural defect candidate images in either a first display area or a second display area according to the defect type of each of the

extracted defect candidate images together with their classified information regarding the first category and the second category, wherein the first display area corresponds to the first category and the second display area corresponds to the second category."

Claims 6 and 9 also include similar but broader limitations.

Again, note that Berezin displays defect information on display (16). Nishimura discloses imaging defects, as illustrated in figure 3, extracting data, as illustrated in figures 7 and 8 with said data being displayed alongside an image of the defect, in this case, a "bump". See also Nishimura, col. 8, lines 30-55 and col. 10, line 55-col. 11, line 37.

Further regarding Claims 1, 6 and 9, Berezin does not expressly disclose, but Baker discloses displaying on a screen, various graphical charts and images as well as data in linked files and graphical representations, i.e., various first and second or even third display areas together with classified information regarding the first and second categories, as illustrated in Baker at figures 6, 20, and 23-28. See also discussion at Baker, col. 3, lines 18-40, col. 15, lines 10-21, col. 16, line 55-col. 17, line 30.

Note that Nishimura discloses at figure 3, the classifying of various defect images with various ideal defect and non-defect images along with a defect name. See also figures 7 and 8 which further discloses linking graphical data with an ideal image of a particular defect.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to have included extracted defect image data alongside various ideal pattern images as well as graphical representations of data such as wafer maps, histograms

and the like, on several areas of a display screen for the purpose of efficiently organizing data necessary for semiconductor defect analysis. See Baker, col. 3, lines 10-40. Further, one ordinarily skilled in the art would recognize that including the defect image along with the graphical numerical data, a representation of an ideal defect, as well as classification data would aid in a quality analysis of a semiconductor process. Such an ordinarily skilled person would then be led by Berezin's disclosure with regards to analysis of semiconductor defect data, along with Baker's teaching of combining several types of semiconductor defect data together for efficient access to the analyst, as well as Nishimura's teaching in figure 3 of locating defect images (dark field illuminated) next to ideal defect images (sectional view of bumps) as well as classification data, i.e., “kinds of faults."

Response to Arguments

3. Applicant's arguments filed 10/29/07 have been fully considered but they are not persuasive. See discussion, above.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yoshida '765, Shibata '469, Hennessey '787, Tanaka '563 and Takagi '965 are all cited as examples of semiconductor defect imaging apparatus.

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY A. SHAPIRO whose telephone number is (571)272-6943. The examiner can normally be reached on Monday-Friday, 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick H. Mackey can be reached on (571)272-6916. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. A. S./
Examiner, Art Unit 3653

/Patrick H. Mackey/
Supervisory Patent Examiner, Art Unit 3653

February 2, 2008